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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,584	09/30/2003	Erik C. Cota-Robles	42P10795	7969

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EXAMINER	
CHOE, YONG J	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/676,584	COTA-ROBLES ET AL.	
	Examiner	Art Unit	
	Yong Choe	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/30/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,25,27,28,34-56,62,63,69 and 79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,34-54 and 69-79* is/are rejected.

7)☒ Claim(s) *20,21,25,27,28,55,56,62 and 63* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *see attached PTO-1449*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/676584 has a total of 60 claims pending in the application. There are 3 independent claims (e.g., claim 1,36 and 71) and 35 dependent claims, all of which are ready for examination by the examiner.

Priority

2. As required by M.P.E.P. 201.14(c), acknowledgment is made of applicant's claim for priority based on an application filed on 10/25/2004.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Drawings

4. The drawings submitted on 09/30/2003 are acceptable for examination purposes.

Specification

5. The disclosure is objected to because of the following informalities:

The specification is objected to as failing to comply with 37 CFR 1.77 (b) because the specification did not include the BRIEF SUMMARY OF THE INVENTION.

Appropriate correction is required.

Claim Objections

6. Claims 1,2,6,9,12,35-37,44,49,52,55,62,69-72 and 79 are objected to because of the following informalities:

- Regarding claims 1,2,36,37,71 and 72, IA-32 should be spelled out at its first use.
- Regarding claims 6,9,12,35,44,49,52,55,62,69 and 79, TLBVMX should be spelled out at its first use.
- Regarding claims 35 and 70, CPUID should be spelled out at its first use.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Regarding claims 1,2,35,36,37,70,71 and 72, the claim scope is uncertain since the trademark or trade name, "Intel" (IA-32 = Intel Architecture processor) cannot be used properly to identify any particular material or product. See MPEP § 2173.05(u).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1-19,34-54 and 69-79** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chauvel (US Patent No.: 6,839,813)** in view of **Long et al. (US Patent No.: 6,674,536)**.

Regarding independent claims 1,36 and 71, Chauvel discloses an apparatus comprising: a translation lookaside buffer (TLB) (Fig.6: i.e., TLB 2130) in a processor having a plurality of TLB entries (Fig.6: entries in TLB 2130), each TLB entry (Fig.6: entries in TLB 2130) being associated with a virtual machine extension (VMX) tag word (Fig.4: i.e., control word 402); indicating if the associated TLB entry (Fig.6: entries in TLB 2130) is invalidated according to a processor mode, when an invalidation operation (col.13, lines 56-64: "invalidate entry" operation) is performed; the processor mode being one of execution in a virtual machine (VM) and execution not in a virtual machine (col.13, lines 56-64 and col.16, lines 18-29 and claim 2 and TABLE 5);

However, Chauvel does not specifically teach the invalidation operation belonging to a non-empty set of invalidation operations composed of a union of (1) a possibly empty set of operations that invalidate a variable number of TLB entries, (2) a possibly empty set of operations that invalidate exactly one TLB entry, (3) a possibly empty set of operations that invalidate the plurality of TLB entries, (4) a possibly empty set of operations that enable and disable use of virtual memory, and (5) a possibly empty set of operations that configure physical address size, page size or other virtual

memory system behavior in a manner that changes the manner in which a physical machine interprets the TLB entries;

wherein the invalidation operations include IA-32speciic operations (a) IA-32 task switches involving changes of virtual memory related control registers, or (b) loading of control registers that modify IA-32 specific page size extension (SPE) and physical address extension (PAE).

Long et al. teaches the invalidation operation belonging to a non-empty set of invalidation operations composed of a union of (1) a possibly empty set of operations that invalidate a variable number of TLB entries, (2) a possibly empty set of operations that invalidate exactly one TLB entry, (3) a possibly empty set of operations that invalidate the plurality of TLB entries, (4) a possibly empty set of operations that enable and disable use of virtual memory, and (5) a possibly empty set of operations that configure physical address size, page size or other virtual memory system behavior in a manner that changes the manner in which a physical machine interprets the TLB entries (col.117, lines 8-35).

wherein the invalidation operations include IA-32speciic operations (a) IA-32 task switches involving changes of virtual memory related control registers, or (b) loading of control registers that modify IA-32 specific page size extension (SPE) and physical address extension (PAE) (col.119, lines 19-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the invalidation operation as taught by Long et al. into the TLB of Chauvel in order to perform a different calculation (col.2, line 28).

Therefore, it would have been obvious to combine the invalidation operation as taught by Long et al. with the TLB of Chauvel to obtain the invention.

Regarding claims 2,37 and 72, Long teaches wherein the invalidation operation is one of (1) a loading of a first control register conditioned on a global bit, (2) an execution of a page invalidate instruction, (3) an IA-32 task switch involving change of at least one virtual memory related control register (4) a loading of a second control register that modifies one of a protected mode indicator and a page mode indicator, and (5) a loading of a third control register that modifies one of an IA-32-specific page size extension (PSE), a page global enable (PGE), and a physical address extension (PAE) (col.119, lines 19-28).

Regarding claims 3,38 and 73, Chauvel teaches wherein the processor is in or not in VMX mode and the TLB entry is not invalidated at loading of the first control register when one of a transition into VMX mode (a VM entrance) and a transition out of VMX mode (a VM exit) occurs (col.13, lines 56-64).

Regarding claims 4,39 and 74, Chauvel teaches wherein the VMX tag word is a single bit and the VMX tag word is negated for a new TLB entry when the processor is not in VMX mode and the VMX tag word is asserted for a new TLB entry when the processor is in VMX mode; and the TLB entry is invalidated when an invalidation operation is performed and the VMX tag word is asserted and the processor is in VMX mode (col.13, lines 7-13).

Regarding claims 5,8,40,43,75 and 78, Chauvel teaches wherein the TLB entry is invalidated irrespective of value of the VMX tag word when an invalidation operation is performed and the processor is not in VMX mode (col.13, lines 56-64).

Regarding claims 6,9,41,44,76 and 79, Chauvel teaches wherein a field in a control register is designated the translation lookaside buffer virtual machine extension (TLBVMX) word and the TLB entry is invalidated when an invalidation operation is performed and the VMX tag word matches the TLBVMX word and the processor is not in VMX mode (col.13, lines 7-13).

Regarding claims 7,42 and 77, Chauvel teaches wherein the VMX tag word is a single bit and the VMX tag word is asserted for a new TLB entry when the processor is not in VMX mode and the VMX tag word is negated for a new TLB entry when the processor is in VMX mode; and the TLB entry is invalidated when an invalidation operation is performed and the VMX tag word is negated and the processor is in VMX mode (col.13, lines 7-13).

Regarding claims 10 and 45, Chauvel teaches wherein invalidation of a TLB entry by an invalidation operation is further conditioned upon value of one or more control words associated with the TLB (col.13, lines 7-13).

Regarding claims 11 and 46, Chauvel teaches wherein the control word or words associated with the TLB are located in one or more of the control registers of the processor or in a Virtual Machine Control Structure (VMCS) in memory (col.13, lines 22,31).

Regarding claims 12 and 47, The apparatus of claim 11 wherein one of the control words associated with the TLB is distinguished such that the VMX tag word is set to match a distinguished control word for a new TLB entry, the distinguished control word associated with the TLB being designated the TLBVMX word (col.5, lines 18-29).

Regarding claims 13 and 48, Chauvel teaches wherein the TLBVMX word is set to one of a plurality of values that constitute a proper subset of a set of all possible values for a VMX tag word when the processor mode corresponds to execution in a virtual machine (VM) (see table 5 and col.16, lines 18-28).

Regarding claims 14 and 49, Chauvel teaches wherein the TLB entry is invalidated when an invalidation operation is performed and the value of the associated VMX tag word matches the value of the TLBVMX word and the processor mode corresponds to execution in a virtual machine (VM) (col.13, lines 65-67 and col.14, lines 1-10).

Regarding claims 15 and 50, Chauvel teaches wherein the one or more control words associated with the TLB, including the TLBVMX word, are configurable when the processor mode corresponds to execution not in a virtual machine (col.13, lines 7-13).

Regarding claims 16 and 51, Long teaches wherein the TLBVMX word is set to one of a plurality of values that constitute a proper subset of a set of all possible values for a VMX tag word when the processor mode corresponds to execution not in a virtual machine (col.117, lines 8-35).

Regarding claims 17 and 52, Chauvel teaches wherein a set theoretic intersection of the plurality of values allowable for the TLBVMX word when the

processor mode corresponds to execution not in a virtual machine and the plurality of values allowable for the TLBVMX word when the processor mode corresponds to execution in a virtual machine (VM) is an empty set (col.13, lines 7-13).

Regarding claims 18 and 53, Long teaches wherein invalidation of a TLB entry by an invalidation operation is further conditioned upon value of a second control word associated with the TLB when the processor mode corresponds to execution not in a virtual machine (col.117, lines 8-35).

Regarding claims 19 and 54, Chauvel teaches wherein the TLB entry is invalidated when an invalidation operation is performed and the associated VMX tag word matches the second control word associated with the TLB and the processor mode corresponds to execution not in a virtual machine (col.13, lines 7-13).

Regarding claims 34 and 69, Chauvel teaches wherein size of a VMX tag word and the TLBVMX word is determined by executing a specified processor instruction in a specified manner (col.13, lines 7-13).

Regarding claims 35 and 70, Chauvel teaches wherein the processor is compatible with the Intel Architecture and the specified instruction is a CPUID instruction and the specified manner is to have a specified value in an EAX register when the CPUID instruction is executed (col.6, lines 34-35 and Wikipedia also teaches that the CPUID opcode is an instruction (its name derived from CPU IDentification) for the x86 architecture. It was introduced by Intel in the early 1990s for later steppings of the 486 chip, and fully rolled out at the introduction of the Pentium processor.[1] By using the CPUID opcode, software can determine processor type and the presence of

features (like MMX/SSE). The CPUID opcode is 0FA2h and the value in the EAX register specifies what information to return).

Allowable Subject Matter

11. Claims 20,21,25,27,28,55,56,62 and 63 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form incorporating all of the limitations of the base claims 1 and 36 respectively and a including all of the limitations of the base claims and any intervening claims.

Conclusion

12. Claims rejected in the application

Per the instant office action, claims 1-21,25,27,28,34-56,62,63,69 and 79 have received a first action on the merits and are subject of a first action non-final.

13. Any inquiry concerning this communication should be directed to **Yong Choe** at telephone number **571-270-1053**. The examiner can normally be reached on M-F 8:00am to 5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Sanjiv Shah** can be reached on **571-272-4098**. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-irect.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER

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